

WHAT IS CLAIMED IS:

1. A disk controller for controlling reading and writing of data from and to a disk, comprising:

5 a first terminal used to output a first write gate signal which dictates writing of data to the disk;

a second terminal used to input a second write gate signal output from an external circuit, the external circuit performing predetermined signal processing on write data in accordance with the first write gate signal output from the first terminal, and outputting the second write gate signal, the second write gate signal reflecting a signal delay in the predetermined signal processing; and

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15 a write inhibition controller which monitors the second write gate signal input via the second terminal, and detects, as a write inhibition state, a state in which writing of data to the disk is dictated during a period in which writing of data to the disk should be inhibited.

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2. The disk controller according to claim 1, wherein:

the external circuit is a signal processing circuit, the signal processing circuit performing the signal processing on write data in accordance with the first write gate signal output from the first terminal, and outputting the processed write data to a

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head amplifier circuit, the signal processing circuit
also outputting the second write gate signal, a period
in which the second write gate signal is valid being
longer, by a time corresponding to a delay time in the
5 predetermined signal processing, than a period in
which the first write gate signal is valid, the head
amplifier circuit causing a head to read or write data
from or to the disk; and

the second terminal is used to input the second
10 write gate signal output from the signal processing
circuit.

3. The disk controller according to claim 2,
further comprising a read/write controller which
outputs a third write gate signal, together with the
15 write data used in the predetermined signal processing
by the signal processing circuit, the third write gate
signal being used as the first write gate signal
output from the first terminal.

4. The disk controller according to claim 3,
20 wherein the write inhibition controller outputs the
second write gate signal as a fourth write gate signal
in a normal state, without changing a state of the
second write gate signal, the write inhibition
controller negating the second write gate signal and
25 outputting the negated second write gate signal as the
fourth write gate signal in the write inhibition
state, the fourth write gate signal being used to

instruct the head amplifier circuit to write data to the disk.

5 5. The disk controller according to claim 4, further comprising a third terminal used to output, to an outside of the disk controller, the fourth write gate signal supplied from the write inhibition controller.

10 6. The disk controller according to claim 5, wherein the third terminal is used to output, to the head amplifier circuit, the fourth write gate signal supplied from the write inhibition controller.

7. The disk controller according to claim 2, further comprising:

15 a read/write controller which outputs a third write gate signal used as the first write gate signal output from the first terminal, together with the write data used in the predetermined signal processing by the signal processing circuit, the read/write controller causing the third write gate signal not to
20 reflect a signal delay in the signal processing circuit in the first mode, and causing the third write gate signal to reflect a signal delay in the signal processing circuit in the second mode; and

25 a monitoring target selection circuit which selects one of the second and third write gate signals to be monitored by the write inhibition controller, the monitoring target selection circuit selecting, in

the first mode, the second write gate signal input via the second terminal, and selecting, in the second mode, the third write gate signal output from the read/write controller, and

5 wherein the write inhibition controller detects the write inhibition state by monitoring the second write gate signal in the first mode, and monitoring the third write gate in the second mode.

8. The disk controller according to claim 7,
10 wherein the monitoring target selection circuit includes:

 a first switch which transmits, to the write inhibition controller, the third write gate signal output from the read/write controller, the first
15 switch being open in the first mode and closed in the second mode; and

 a second switch which transmits, to the write inhibition controller, the second write gate signal input via the second terminal, the second switch being
20 closed in the first mode and open in the second mode.

9. The disk controller according to claim 8, further comprising:

 a third terminal used to output a fourth write gate signal to an outside of the disk controller in
25 the first mode; and

 a multiplexer which selects the third write gate signal, output from the read/write controller, as the

first write gate signal in the first mode, and selects a fifth write gate signal as the first write gate signal in the second mode, and

wherein:

5 in the first mode, the write inhibition controller outputs the second write gate signal as the fourth write gate signal in a normal state, without changing a state of the second write gate signal, the write inhibition controller negating the second write
10 gate signal and outputting the negated second write gate signal as the fourth write gate signal in the write inhibition state; and

 in the second mode, the write inhibition controller outputs the third write gate signal as the
15 fifth write gate signal in the normal state, without changing a state of the third write gate signal, the write inhibition controller negating the third write gate signal and outputting the negated third write gate signal as the fifth write gate signal in the
20 write inhibition state.

10. The disk controller according to claim 7, wherein the monitoring target selection circuit includes a multiplexer which selects, in the first mode, the second write gate signal input via the
25 second terminal, and selects, in the second mode, the third write gate signal output from the read/write controller, the signal selected by the multiplexer

being transmitted to the write inhibition controller.

11. The disk controller according to claim 7,
further comprising:

5 a third terminal used to output a fourth write
gate signal to an outside of the disk controller in
the first mode; and

a first multiplexer which selects the third write
gate signal, output from the read/write controller, as
the first write gate signal in the first mode, and
10 selects a fifth write gate signal as the first write
gate signal in the second mode, and

wherein:

the monitoring target selection circuit includes
a second multiplexer which selects, in the first mode,
15 the second write gate signal input via the second
terminal, and selects, in the second mode, the third
write gate signal output from the read/write
controller, the signal selected by the second
multiplexer being transmitted to the write inhibition
20 controller; and

the write inhibition controller includes a write
gate signal output port used to output the fourth
write gate signal in the first mode and output the
fifth write gate in the second mode,

25 in the first mode, the write inhibition
controller outputting the second write gate signal,
selected by the second multiplexer, as the fourth

write gate signal in a normal state through the write gate signal output port, without changing a state of the second write gate signal, the write inhibition controller negating the second write gate signal and outputting the negated second write gate signal as the fourth write gate signal through the write gate signal output port in the write inhibition state, and

in the second mode, the write inhibition controller outputting the third write gate signal, selected by the second multiplexer, as the fifth write gate signal in the normal state through the write gate signal output port, without changing a state of the third write gate signal, the write inhibition controller negating the third write gate signal and outputting the negated third write gate signal as the fifth write gate signal through the write gate signal output port in the write inhibition state.

12. The disk controller according to claim 11, further comprising an output destination-switching unit which outputs, to the third terminal in the first mode, the fourth write gate signal output from the write gate signal output port of the write inhibition controller, and outputs, to the first multiplexer in the second mode, the fifth write gate signal output from the write gate signal output port of the write inhibition controller.

13. The disk controller according to claim 7,

further comprising:

a third terminal used to output a fourth write gate signal to an outside of the disk controller in the first mode; and

5 an external output target selection circuit which selects the third write gate signal, output from the read/write controller, as the first write gate signal in the first mode, and selects a fifth write gate signal as the first write gate signal in the second
10 mode, and

wherein:

in the first mode, the write inhibition controller outputs the second write gate signal as the fourth write gate signal in a normal state, without
15 changing a state of the second write gate signal, the write inhibition controller negating the second write gate signal and outputting the negated second write gate signal as the fourth write gate signal in the write inhibition state, and

20 in the second mode, the write inhibition controller outputs the third write gate signal as the fifth write gate signal in the normal state, without changing a state of the third write gate signal, the write inhibition controller negating the third write
25 gate signal and outputting the negated third write gate signal as the fifth write gate signal in the write inhibition state.

14. The disk controller according to claim 13,
wherein the third terminal is used in the first mode
to output, to the head amplifier circuit, the fourth
write gate signal supplied from the write inhibition
5 controller.

15. The disk controller according to claim 14,
wherein the disk controller is used in the first mode
if the signal processing circuit is a first signal
processing circuit, and used in the second mode if
10 the signal processing circuit is a second signal
processing circuit, the first signal processing
circuit performing predetermined signal processing on
write data in accordance with the first write gate
signal output through the first terminal, the first
15 signal processing circuit outputting the second write
gate signal, a valid period of the second write gate
signal being longer than the first write gate signal
by a time corresponding to a delay time in the
predetermined signal processing, the second signal
20 processing circuit outputting the second write gate
signal, the second signal processing circuit being
unable to output the second write gate signal, and
performing predetermined signal processing on write
data in accordance with the first write gate signal
25 output through the first terminal.

16. The disk controller according to claim 15,
wherein the first terminal is used in the first mode

to output the first write gate signal to the first
signal processing circuit, and used in the second mode
to output the first write gate signal to the second
signal processing circuit and the head amplifier
5 circuit.

17. The disk controller according to claim 1,
wherein the disk is provided with a plurality of servo
areas extending radially at circumferentially regular
intervals, and a period in which writing of data to
10 the disk should be inhibited corresponds to a period
in which a head is passing through one of the
plurality of servo areas.

18. The disk controller according to claim 1,
wherein the disk is rotated by a spindle motor, and
15 a period in which writing of data to the disk should
be inhibited corresponds to a period in which a
rotational speed of the spindle motor is in a non-
steady state.

19. A disk drive comprising:
20 a disk controller for controlling reading and
writing of data from and to a disk, the disk
controller including:

a first terminal used to output a first
write gate signal which dictates writing of data to
25 the disk;

a second terminal used to input a second
write gate signal;

a read/write controller which outputs,
together with write data, a third write gate signal
used as the first write gate signal output through the
first terminal;

5 a third terminal used to output a fourth
write gate signal to an outside of the disk
controller; and

a write inhibition controller which monitors
the second write gate signal input via the second
10 terminal, and detects, as a write inhibition state, a
state in which writing of data to the disk is dictated
during a period in which writing of data to the disk
should be inhibited, the write inhibition controller
outputting the second write gate signal as the fourth
15 write gate signal in a normal state without changing a
state of the second write gate signal, the write
inhibition controller negating the second write gate
signal and outputting the negated second write gate
signal as the fourth write gate signal in the write
20 inhibition state;

a signal processing circuit connected to the disk
controller via the first and second terminals of the
disk controller, the signal processing circuit
performing predetermined signal processing on write
25 data in accordance with the first write gate signal
output through the first terminal, and outputting the
second write gate signal, a valid period of the second

write gate signal being longer than the first write gate signal by a time corresponding to a delay time in the predetermined signal processing; and

5 a head amplifier circuit which causes a head to write, to the disk, the write data processed by the signal processing circuit in accordance with the fourth write gate signal output through the third terminal of the disk controller.

20. A method of controlling inhibition of writing
10 of data to a disk, for use in a disk drive in which reading and writing of data from and to the disk is performed using a head under control of a disk controller via a signal processing circuit and a head amplifier circuit, the method comprising:

15 outputting a first write gate signal and write data from the disk controller to the signal processing circuit, the first write gate signal instructing the signal processing circuit to write the write data;

performing predetermined signal processing on the
20 write data in accordance with the first write gate signal output from the disk controller to the signal processing circuit;

outputting a second write gate signal
corresponding to the first write gate signal from the
25 signal processing circuit to the disk controller, the second write gate signal reflecting a signal delay in the predetermined signal processing;

detecting, as a write inhibition state, a state in which an instruction to write data to the disk is issued during a period in which writing of data to the disk should be inhibited, in accordance with the

5 second write gate signal output from the signal processing circuit to the disk controller; and

outputting, from the disk controller to the head amplifier circuit, the second write gate signal as a fourth write gate signal in a normal state, without
10 changing a state of the second write gate signal, the fourth write gate signal instructing writing, to the disk, of the write data processed by the signal processing circuit; and

negating the second write gate signal in the
15 write inhibition state, and outputting, from the disk controller to the head amplifier circuit, the negated second write gate signal as the fourth write gate signal in the write inhibition state.